IP-DIO32

32 CHANNEL INPUT/OUTPUT
Industry Pack Module
HARDWARE REFERENCE MANUAL

Revision 1.8
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Revision 1.4 change : Made change to I/O space register map.
Revision 1.5 change : Made change to ID space map.
Revision 1.6 change : Corrected resistor and voltage data, added examples.
Revision 1.7 change : Corrected equation and added examples for page 19
Revision 1.8 change : Updated for Rev B PWB. Jumper correction page 26

1 Introduction

1.1 Functional description

The IP_DIO32 module has 32 INPUT/OUTPUT channels configured as four 8-bit ports that can be programmed as Input or Output.

Key Features are:

- Up to 32 I/O Pin available by group of 8
- Direct read-back outputs
- Open drain VMOS that can sink up to 100mA at voltage up to 40V.
- Very low Ron (0.3Ω) for reduce heat dissipation
- Pull –Up resistor with +5v internal or variable external reference jumper selected
- Wide input range from 0V to 30V
- Hysteresis on each channel
- Variable threshold can be changed by change of network
- Threshold source can be internal or external selected by jumper
- Change of state detection can generate IP Interrupt
- Integrated Altera logic for Custom option
- 8 or 32 MHz IPCLK

2 MAP ADDRESS

The IP_DIO32 module uses the three available spaces defined in the Industries Pack specifications.

2.1 IDSPACE

Up to 32 bytes of registered data to provide information about the module to the user. The lower address contains data related to the type of module, revision, etc...
Only even address data are valid.

ID space address	Description	Value
$00	ASCII “I”	$49
$02	ASCII “P”	$50
$04	ASCII “A”	$41
$06	ASCII “C”	$43
$08	Manufacturer identification	$11
$0A	Module type	$16
$0C	Revision module	$0A
$0E	Reserved	$00
$10	Driver ID, low byte	
$12	Driver ID, high byte	
$14	Number of bytes used	$0A
$16	CRC	
$18-$3E	User space	

Table 2-1 IDSEL0 SPACE byte content

2.2 IOSPACE

IP_DIO32 uses the IOSPACE for the following registers. Note: in byte access even address is the lower byte, odd address is upper byte.

Slave Address	NAME	REGISTER	TYPE	R/W
$00	Port [08..01] I/O Configuration	CNFG0H	High	R/W
$01	Port [16..09] I/O Configuration	CNFG0L	Low	R/W
$02	Port [24..17] I/O Configuration	CNFG1H	High	R/W
$03	Port [32..25] I/O Configuration	CNFG1L	Low	R/W
$04	Output Port [08..01] ON/OFF	OUT0H	High	R/W
$05	Output Port [16..09] ON/OFF	OUT0L	Low	R/W
$06	Output Port [24..17] ON/OFF	OUT1H	High	R/W
$07	Output Port [32..25] ON/OFF	OUT1L	Low	R/W
$08	Input Port [08..01] status	RD_INP0H	High	R
$09	Input Port [16..09] status	RD_INP0L	Low	R
$0A	Input Port [24..17] status	RD_INP1H	High	R
$0B	Input Port [32..25] status	RD_INP1L	Low	R
$0C	Input Port [08..01] interrupt enable	INTEN0H	High	R/W
$0D	Input Port [16..09] interrupt enable	INTEN0L	Low	R/W
$0E	Input Port [24..17] interrupt enable	INTEN1H	High	R/W
$0F	Input Port [32..25] interrupt enable	INTEN1L	Low	R/W
$10	Input Port [16..01] interrupt COS	INTPOL0	WORD	R/W
$12	Input Port [32..17] interrupt COS	INTPOL1	WORD	R/W
$14	Input Port [16..01] interrupt pending	RD_INTPEND0	WORD	R
$16	Input Port [32..17] interrupt pending	RD_INTPEND1	WORD	R
$18	Input Port [16..01] interrupt cleared	WR_INTCLR0	WORD	W
$1A	Input Port [32..17] interrupt cleared	WR_INTCLR1	WORD	W
$1D	Interrupt Group (byte) pending	RD_COSR	BYTE	R
$1F	Control Register 0	CTRL0	BYTE	W
$21	Control Register 1	CTRL1	BYTE	W
$23	IVR0 for INTREQ0	IVR0	BYTE	R/W
$25	IVR1 for INTREQ1	IVR1	BYTE	R/W

3 Registers description

3.1 Port I/O Configuration

3.1.1 CNFG0H-CNFG0L (I/O # 16 – 01)

Slave address: IOSPACE + $00-$01(byte access)
Configuration register can be accessed in byte or word.

A ”0” selects the I/O pins as INPUT.
A ”1” selects the I/O pins as OUTPUT.
Register is cleared upon IP RESET.

BD07	BD06	BD05	BD04	BD03	BD02	BD01	BD00
I/O #8	I/O #7	I/O #6	I/O #5	I/O #4	I/O #3	I/O #2	I/O #1

BD15	BD14	BD13	BD12	BD11	BD10	BD09	BD08
I/O #16	I/O #15	I/O #14	I/O #13	I/O #12	I/O #11	I/O #10	I/O #9

3.1.2 CNFG1H-CNFG1L (I/O # 32 – 17)

Slave address: IOSPACE + $02-$03 (byte access)
Configuration register can be accessed in byte or word.

A ”0” selects the I/O pins as INPUT.
A ”1” selects the I/O pins as OUTPUT.
Register is cleared upon IP RESET.

BD07	BD06	BD05	BD04	BD03	BD02	BD01	BD00
I/O #24	I/O #23	I/O #22	I/O #21	I/O #20	I/O #19	I/O #18	I/O #17

BD15	BD14	BD13	BD12	BD11	BD10	BD09	BD08
I/O #32	I/O #31	I/O #30	I/O #29	I/O #28	I/O #27	I/O #26	I/O #25

3.2 OUTPUT PORT

3.2.1 OUT0H-OUT0L (I/O # 16 – 01)

Slave address: IOSPACE + $04-$05 (byte access)
Output port register can be accessed in byte or word.

If I/O channels are selected as OUTPUT, this register controls the output level (On or Off).
A ”0” open drain is “OFF” means NON conductive.
A ”1” open drain is “ON” means conductive. Ron is 0.3Ω.
Writing a “1” or a “0” to a port defined as INPUT has no effect.
IF PORT is selected as an Output, read-back of the register provides the status of the bit written. Writing a “1” will read-back a “1”. This bit controls the VMOS Gate. The VMOS behaves as an inverter. When Gate is “1”, it is conductive and the Drain is close to analog GND or “”0”. A read-back of the **Input Status Register** will provide the level of the Drain Output witch will appear as a “0”.
Register is cleared upon IP RESET.

BD07	BD06	BD05	BD04	BD03	BD02	BD01	BD00
O #8	O #7	O #6	O #5	O #4	O #3	O #2	O #1

BD15	BD14	BD13	BD12	BD11	BD10	BD09	BD08
O #16	O #15	O #14	O #13	O #12	O #11	O #10	O #9

3.2.2 OUT1H-OUT1L (I/O # 32 – 17)

Slave address: IOSPACE + $06-$07 (byte access).
Output port register can be accessed in byte or word.

If I/O channels are selected as OUTPUT, this register controls the output level (On or Off).
A ”0” open drain is “OFF” means NON conductive.
A ”1” open drain is “ON” means conductive. Ron is 0.3Ω.
Writing a “1” or a “0” to a port defined as INPUT has no effect.
IF PORT is selected as an Output, a Read to the location will return the status of the latched data from output port.
Register is cleared upon IP RESET.

BD07	BD06	BD05	BD04	BD03	BD02	BD01	BD00
O #24	O #23	O #22	O #21	O #20	O #19	O #18	O #17

BD15	BD14	BD13	BD12	BD11	BD10	BD09	BD08
O #32	O #31	O #30	O #29	O #28	O #27	O #26	O #25

3.3 INPUT PORT STATUS

3.3.1 RD_INP0H-RD_INP0L (I/O #16 – 01)

Slave address: IOSPACE + $08-$09 (byte access)
Input port status register can be accessed in byte or word.

If I/O channels are selected as INPUT this register gives status of the input level.
Register is cleared upon IP RESET.
If port is selected as an Output, a Read to this location will return the status of the latched data from output port.

BD07	BD06	BD05	BD04	BD03	BD02	BD01	BD00
I #8	I #7	I #6	I #5	I #4	I #3	I #2	I #1

BD15	BD14	BD13	BD12	BD11	BD10	BD09	BD08
I #16	I #15	I #14	I #13	I #12	I #11	I #10	I #9

3.3.2 RD_INP1H-RD_INP1L (I/O #32 – 17)

Slave address: IOSPACE + $0A-$0B (byte access)
Input port status register can be accessed in byte or word.

If I/O channels are selected as INPUT this register gives status of the input level
Register is cleared upon IP RESET.
If port is selected as an Output, a Read to the location will return the status of the latched data from output port.

BD07	BD06	BD05	BD04	BD03	BD02	BD01	BD00
I #24	I #23	I #22	I #21	I #20	I #19	I #18	I #17

BD15	BD14	BD13	BD12	BD11	BD10	BD09	BD08
I #32	I #31	I #30	I #29	I #28	I #27	I #26	I #25

3.4 INPUT PORT INTERRUPT ENABLE

3.4.1 INTEN0H-INTEN0L (I/O #16 – 01)

Slave address: IOSPACE + $0C-$0D (byte access)
Input port interrupt enable register can be accessed in byte or word.

This register enables the corresponding port selected as INPUT to generate an Interrupt IF:

- The corresponding enabled bit associated with the INPUT is set to a “1”.
- Port is selected as INPUT
- IP interrupts INTREQ0 or INTREQ1 are enable

A ”0” disables the port to be a source for Interrupt.
A ”1” enables the port to be the source for Interrupt.
Register is cleared upon IP RESET. All interrupt are disable

BD07	BD06	BD05	BD04	BD03	BD02	BD01	BD00
I #8	I #7	I #6	I #5	I #4	I #3	I #2	I #1

BD15	BD14	BD13	BD12	BD11	BD10	BD09	BD08
I #16	I #15	I #14	I #13	I #12	I #11	I #10	I #9

3.4.2 INTEN1H-INTEN1L (I/O #32 – 17)

Slave address: IOSPACE + $0E-$0F (byte access)
Input port interrupt enable register can be accessed in byte or word.

This register enables the corresponding port selected as INPUT to generate an Interrupt IF:

- The corresponding enabled bit associated with the INPUT is set to a “1”.
- Port is selected as INPUT
- IP interrupts INTREQ0 or INTREQ1 is enable

A ”0” disables the port to be a source for Interrupt.
A ”1” enables the port to be the source for Interrupt.
Register is cleared upon IP RESET. All interrupt are disable

BD07	BD06	BD05	BD04	BD03	BD02	BD01	BD00
I #24	I #23	I #22	I #21	I #20	I #19	I #18	I #17

BD15	BD14	BD13	BD12	BD11	BD10	BD09	BD08
I #32	I #31	I #30	I #29	I #28	I #27	I #26	I #25

3.5 INPUT PORT INTERRUPT COS (Change Of State)

3.5.1 INTPOLH-INTPOL0L (I/O #16 – 01)

Slave address: IOSPACE + $10 (word access).
Input port COS register can be accessed in word only.

This register selects the polarity of the Input Port COS that will generate an interrupt.
A ”0” provides a COS on a raising edge of the Input Port.
A ”1” provides a COS on a falling edge of the Input Port.
Register is cleared upon IP RESET making rising edge default.

BD07	BD06	BD05	BD04	BD03	BD02	BD01	BD00
COS #8	COS #7	COS #6	COS #5	COS #4	COS #3	COS #2	COS #1

BD15	BD14	BD13	BD12	BD11	BD10	BD09	BD08
COS #16	COS #15	COS #14	COS #13	COS #12	COS #11	COS #10	COS #9

3.5.2 INTPOL1H-INTPOL1L (I/O #32 – 17)

Slave address: IOSPACE + $12 (Word access)
Input port COS register can be accessed in word only.

This register selects the polarity of the Input Port COS that will generate an interrupt.
A ”0” provides a COS on a raising edge of the Input Port.
A ”1” provides a COS on a falling edge of the Input Port.
Register is cleared upon IP RESET making rising edge default

BD07	BD06	BD05	BD04	BD03	BD02	BD01	BD00
COS #24	COS #23	COS #22	COS #21	COS #20	COS #19	COS #18	COS #17

BD15	BD14	BD13	BD12	BD11	BD10	BD09	BD08
COS #32	COS #31	COS #30	COS #29	COS #28	COS #27	COS #26	COS #25

3.6 INPUT PORT INTERRUPT PENDING

3.6.1 RD_INTPEND0 (I/O #16 – 01)

Slave address: IOSPACE + $14 (Word access)
Input port Interrupt pending register can be accessed in word only.

Upon receiving an interrupt the host can check the interrupt source:

- At the level of the RD_COSR register.
- By reading registers INTPEND0 or INTPEND1.

A bit read as a "1" will signify that the associated input has change of sign.
Each input is filtered using three (3) IP Clock delays to avoid glitches.
The COS (Change Of State) is latched.
To clear the interrupt write a 1 to the corresponding I/O channel associated with the input source of the interrupt. This will clear the interrupt source. See next register.

BD07	BD06	BD05	BD04	BD03	BD02	BD01	BD00
INPEND #8	INPEND #7	INPEND #6	INPEND #5	INPEND #4	INPEND #3	INPEND #2	INPEND #1

BD15	BD14	BD13	BD12	BD11	BD10	BD09	BD08
INPEND #16	INPEND #15	INPEND #14	INPEND #13	INPEND #12	INPEND #11	INPEND #10	INPEND #9

3.6.2 RD_INTPEND1 (I/O #32 – 17)

Slave address: IOSPACE + $16 (Word access)
Input port Interrupt pending register can be accessed in word only.

Upon receiving an interrupt the host can check the interrupt source:

- At the level of the RD_COSR register.
- By reading registers INTPEND0 or INTPEND1.

A bit read as a "1" will signify that the associated input has change of sign.
Each input is filtered using three (3) IP Clock delays to avoid glitches.
The COS (Change Of State) is then latched.
To clear the interrupt write a 1 to the corresponding I/O channel associated with the input source of the interrupt. This will clear the interrupt source. See next register.

BD07	BD06	BD05	BD04	BD03	BD02	BD01	BD00
INPEN D #24	INPEN D #23	INPEN D #22	INPEN D #21	INPEN D #20	INPEN D #19	INPEN D #18	INPEN D #17

BD15	BD14	BD13	BD12	BD11	BD10	BD09	BD08
INPEN D #32	INPEN D #31	INPEN D #30	INPEN D #29	INPEN D #28	INPEN D #27	INPEN D #26	INPEN D #25

3.7 INPUT PORT INTERRUPT CLEAR

3.7.1 WR_INTCLR0 (I/O #16 – 01)

Slave address: IOSPACE + $18 (Word access)

Input port Interrupt clear register can be accessed in word only.

To clear the interrupt write a 1 to the corresponding I/O channel associated with the input source of the interrupt. This will clear the interrupt source.

BD07	BD06	BD05	BD04	BD03	BD02	BD01	BD00
INTCLR #8	INTCL R #7	INTCL R #6	INTCL R #5	INTCLR #4	INTCL R #3	INTCL R #2	INTCL R #1

BD15	BD14	BD13	BD12	BD11	BD10	BD09	BD08
INTCL R #16	INTCL R #15	INTCL R #14	INTCL R #13	INTCL R #12	INTCL R #11	INTCL R #10	INTCL R #9

3.7.2

3.7.3 WR_INTCLR1 (I/O #32 – 17)

Slave address: IOSPACE + $1A (Word access)
Input port Interrupt clear register can be accessed in word only.

To clear the interrupt write a 1 to the corresponding I/O channel associated with the input source of the interrupt. This will clear the interrupt source.

BD07	BD06	BD05	BD04	BD03	BD02	BD01	BD00
INTCLR #24	INTCL R #23	INTCL R #22	INTCL R #21	INTCLR #20	INTCL R #19	INTCL R #18	INTCL R #17

BD15	BD14	BD13	BD12	BD11	BD10	BD09	BD08
INTCL R #32	INTCL R #31	INTCL R #30	INTCL R #29	INTCL R #28	INTCL R #27	INTCL R #26	INPEN D #25

3.8 INTERRUPT GROUP PENDING

Slave address: IOSPACE + $1D (byte access)
Interrupt group pending register can be accessed in byte or word.

Upon receiving an interrupt the host can check the interrupt source at the level of the RD_COSR register. This register has divided all 32 I/O channels into 4 groups. A “1” represents an interrupt that is pending or is not cleared. Read chart below to interpret.

BD07	BD06	BD05	BD04	BD03	BD02	BD01	BD00
				COS OUT 3 32-25	COS OUT 2 24-17	COS OUT 1 16-09	COS OUT 0 08-01

3.9 CONTROL REGISTER

3.9.1 CTRL0

Slave address: IOSPACE + $1F (byte access)
Control register can be accessed in byte or word.

Only the two lower bits are used to enable IP interrupt #0 or #1

BD07	BD06	BD05	BD04	BD03	BD02	BD01	BD00
						INTREQ#1 ENABLE	INTREQ#0 ENABLE

3.9.2 CTRL1

Slave address: IOSPACE + $21 (byte access)
Control register can be accessed in byte or word.

ANY WRITE TO THIS LOCATION WILL RESET ALL LOCAL REGISTER,SAME AS A POWER–ON RESET.

3.10 INTERRUPT VECTOR REGISTER

3.10.1 IVR0 Interrupt Vector Register

Slave address: IOSPACE + $23 (byte access)
Interrupt Vector register can be accessed in byte only.

This eight-bit register can be read and written to by the host carrier module. The vector is automatically provided upon INTSPACE cycle performed by the Host.

3.10.2 IVR1 Interrupt Vector Register

Slave address: IOSPACE + $25 (byte access)
Interrupt Vector register can be accessed in byte only.

This eight-bit register can be read and written to by the host carrier module. The vector is automatically provided upon INTSPACE cycle performed by the Host.

3.10.3 Interrupt Programming procedure

The following is a step by step explanation on how to program the IP-DIO32 input channel to generate an interrupt. Please follow each step precisely to insure correct execution.

1. **Disable INTREQ-0 and INTREQ-1:** The purpose of starting with disabling the INTREQ-0 and INTREQ-1 is to insure that there is no possibility of generating an interrupt during the programming cycle. To do this perform the following.
    - Write to the **CTRL0 register** the value $00
    - Now INTREQ-0 and INTREQ-1 are cleared.
2. **Enable Interrupt Input Source:** Now choose the input I/O channel you wish to use as the source to trigger your interrupt. To do this perform the following.
    - Write to the **Input port interrupt enable register** the value of the channel you wish. For this example we will use I/O channel # 1, write $0001. See Input port interrupt enable register for further explanation of channels.
    - Now I/O channel # 1 is set as source to trigger an interrupt.
3. **Enable COS (Change of State):** The purpose of this register is to identify whether the Input I/O trigger source will be a rising edge or falling edge to generate the interrupt. To do this perform the following.
    - Write to the **Input port interrupt COS register** either $0000 or $0001 based on the explanation below. For our example we will use a falling edge on the I/O channel #1 to generate an interrupt to do so write $0001. Now the I/O channel #1 is set to trigger an interrupt when the input signal on channel #1 falls below .8 volts.
    - A ”0” provides a COS on a raising edge of the Input Port.
    - A ”1” provides a COS on a falling edge of the Input Port.
4. **Clear INTREQ-0 and INTREQ-1:** The purpose of this step is to prevent the possibility of an interrupt already being active low or in a pending state. You will now write a 1 to the corresponding I/O input channel bit, this well send a clear to that channel. To do this perform the following. For further explanation look up the Input port interrupt clear register.
    - Write to the **Input port interrupt clear register** $0001, this will access I/O input channel #1 and clear any interrupts by sending the signal high.
5. **Enable INTREQ-0 and INTREQ-1:** Now choose which interrupt (INTREQ-0 or **I**NTREQ-1) you would like to activate when I/O Input channel #1 is sent below 0.8 volts then generating an interrupt. To do this, perform the following.
    - Write to the CTRL0 register either of the following
    - INTREQ-0 write a $01
    - INTREQ-1 write a $02
    - For our example write $01 to the CTRL0 register and this will set INTREQ-0 as your interrupt.

To complete this procedure you will verify your programming is correct. To do so simply ground the I/O Input channel #1. To verify it worked make a read of the Input port Interrupt pending register. You should see the corresponding bit of the source I/O channel high if it’s 0 then the interrupt didn’t activate. This concludes the procedure.

4 IP bus interface

		P4		
Pin 1	GND		Pin 26	GND
Pin 2	+5V		Pin 27	+5V
Pin 3	IPRESET*		Pin 28	IPRW*
Pin 4	XLD00		Pin 29	IDSEL0*
Pin 5	XLD01		Pin 30	DMAREQ0*
Pin 6	XLD02		Pin 31	MEMSEL0*
Pin 7	XLD03		Pin 32	DMAREQ1*
Pin 8	XLD04		Pin 33	INTESEL0*
Pin 9	XLD05		Pin 34	DMACK*
Pin 10	XLD06		Pin 35	IOSEL0*
Pin 11	XLD07		Pin 36	
Pin 12	XLD08		Pin 37	XLA01
Pin 13	XLD09		Pin 38	DMAEND*
Pin 14	XLD10		Pin 39	XLA02
Pin 15	XLD11		Pin 40	ERROR*
Pin 16	XLD12		Pin 41	XLA03
Pin 17	XLD13		Pin 42	INTREQ0*
Pin 18	XLD14		Pin 43	XLA04
Pin 19	XLD15		Pin 44	INTREQ1*
Pin 20	IPBS0*		Pin 45	XLA05
Pin 21	IPBS1*		Pin 46	STROBE*
Pin 22			Pin 47	XLA06
Pin 23			Pin 48	IPACK*
Pin 24	+5V		Pin 49	+5V
Pin 25	GND		Pin 50	GND

Table 4 IPBUS connector

4.1 I/O Port

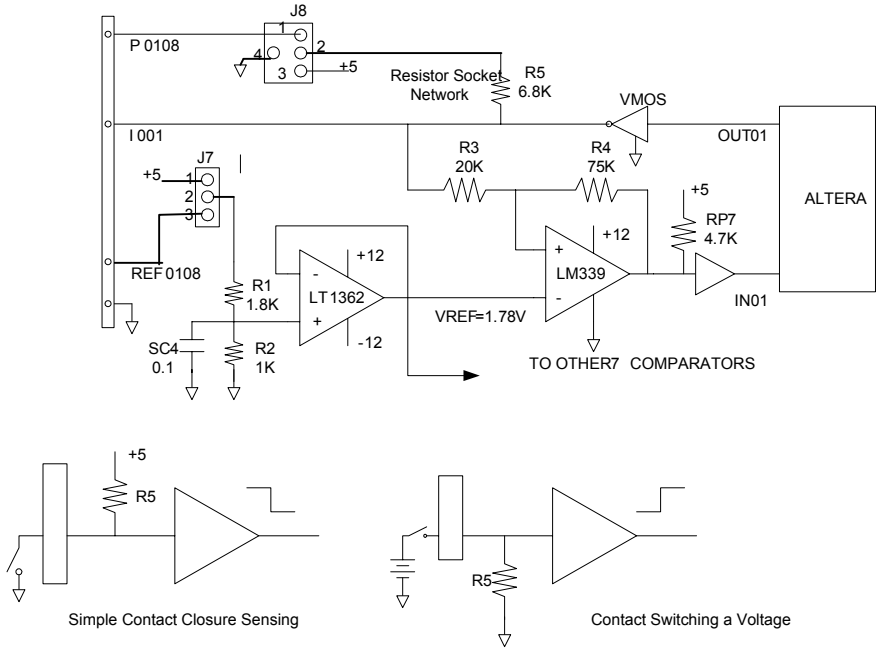
PIN	I/O	PIN	I/O
Pin 1	I/O 01	Pin 26	I/O 05
Pin 2	I/O 02	Pin 27	I/O06
Pin 3	I/O 03	Pin 28	I/O 07
Pin 4	I/O 04	Pin 29	I/O 08
Pin 5	GND	Pin 30	GND
Pin 6	REF0108	Pin 31	P_0108
Pin 7	I/O 09	Pin 32	I/O 13
Pin 8	I/O 10	Pin 33	I/O 14
Pin 9	I/O 11	Pin 34	I/O 15
Pin 10	I/O 12	Pin 35	I/O 16
Pin 11	GND	Pin 36	GND
Pin 12	REF0916	Pin 37	P_0916
Pin 13	I/O 17	Pin 38	I/O 21
Pin 14	I/O 18	Pin 39	I/O 22
Pin 15	I/O 19	Pin 40	I/O 23
Pin 16	I/O 20	Pin 41	I/O 24
Pin 17	GND	Pin 42	GND
Pin 18	REF1724	Pin 43	P_1724
Pin 19	I/O 25	Pin 44	I/O 29
Pin 20	I/O 26	Pin 45	I/O 30
Pin 21	I/O 27	Pin 46	I/O 31
Pin 22	I/O 28	Pin 47	I/O 32
Pin 23	GND	Pin 48	GND
Pin 24	REF2532	Pin 49	P_2532
Pin 25	GND	Pin 50	GND

Table 2 I/O PORT

5 TECHNICAL INFORMATION

5.1 INPUT

An I/O PORT selected as input uses a comparator to provide a TTL signal from the input signal with wide amplitude up to 30Volts.



The reference threshold of the comparator connected to the negative input (-) is provided by a network divider R1, R2 which reference is normally the +5volts. External reference can be selected by a means of jumper.

With R1= 1.8KΩ and R2 = 1KΩ threshold is equal to:

VREF * R2/R1+R2 or 5V * 1KΩ/ (1.8KΩ +1KΩ) = 1.78 Volt

Input signal is connected to the positive input of the comparator through a resistance R3. A positive feedback resistance R4 provides a hysteresis level. The output of the comparator provides a 0 to +5volt signal.

Example for 5V Internal Reference:

Threshold level = VREF * R2/R1+R2 or 5V * 1KΩ/ (1.8KΩ +1KΩ) = 1.78 Volt
R3 = 20 KΩ and
R4 = 75 KΩ,
Hysteresis can be calculated as follows:
High to Low Transition:
Input signal has already provided a +5V output, to toggle input signal should be
(Output signal - Threshold level) / R4 = - (Input signal - Threshold level)/R3
or
(5V-1.78V) / 75 KΩ = (1.78V - Input signal) / 20 KΩ
Input signal =1.78V - (3.22V / 75 KΩ) * 20 KΩ =➔ 0.922V.

Low to High Transition:

To toggle back to a +5V output input signal will be:
Input signal = 1.78V + (1.78V / 75 KΩ) * 20 KΩ =➔ 2.254V.

Example for 15V External Reference:

Threshold level = VREF * R2/R1+R2 or 15V * 1KΩ/ (1.8KΩ +1KΩ) = 5.357 Volt
R3 = 20 KΩ and
R4 = 75 KΩ,
Hysteresis can be calculated as follows:
High to Low Transition:
Input signal has already provided a +5V output, to toggle input signal should be
(Output signal - Threshold level) / R4 = - (Input signal - Threshold level)/R3
or
(5V-5.357V) / 75 KΩ = (5.357 - Input signal) / 20 KΩ
Input signal =5.357V - (-0.357V / 75 KΩ) * 20 KΩ =➔ 5.452V. (Measured 5.2V)

Low to High Transition:

To toggle back to a +5V output input signal will be:
Input signal = 5.357V + (5.357V / 75 KΩ) * 20 KΩ =➔ 6.78V. (Measured 6.7V)

Note: The output of the Comparator is 5.2V Measured

Example for 28V External Reference:

Threshold level = VREF * R2/R1+R2 or 28V * 1KΩ/ (1.8KΩ +1KΩ) = 10 Volt
R3 = 20 KΩ and

R4 = 75 KΩ,
Hysteresis can be calculated as follows:
High to Low Transition:
Input signal has already provided a +5V output, to toggle input signal should be
(Output signal - Threshold level) / R4 = - (Input signal - Threshold level)/R3
or
(5V-10V) / 75 KΩ = (10 - Input signal) / 20 KΩ
Input signal =10V - (-5V / 75 KΩ) * 20 KΩ =➔ 11.33V. (Measured 11.1V)

Low to High Transition:

To toggle back to a +5V output input signal will be:
Input signal = 10V + (10V / 75 KΩ) * 20 KΩ =➔ 12.66V. (Measured 12.7V)

Note: The output of the Comparator is 5.4V Measured

An optional pull-up resistance R5 can be connected by jumper to the +5V, GND or External Pull-up voltage. Depending of the configuration selected, the input Port can be used to:

- Detect a closure between Input Port and GND if pull-up is connected to the +5V.
- Detect a positive voltage transition if the Pull-up is connected to GND.

A resistor network, on a socket, is used for each group of 8.
Default value is 4.7 KΩ, with 1/8 W of maximum power dissipation.

5.2 OUTPUT

Port selected as an output is driven by a VMOS component
Principal characteristics are:

VDS max : 50V
RDS on : 0.3Ω

The same optional pull-up resistance R5 network can be used as a pull-up resistance if the output is to be used to control TTL-level logic.

5.3 I/O CHANNEL CONFIGURATION EXAMPLES

Upon reset the I/O lines are configured as input. The VMOS inverter is “off”, in high impedance mode since its control signal (OUT1) is in a “0” level at reset.

Default configuration: J8: 2-3, J7: 1-2

J8
Is used to provide an internal pull-up voltage for the I/O line when it is used as an input 2-3 will provide 5 Volt pull-up allowing TTL-level outputs, while 2-4 will connect it to ground and 1-2 will provide the External Voltage provided

J7
The comparator has a threshold level that is defined by an internal reference or external reference.

Internal Reference:

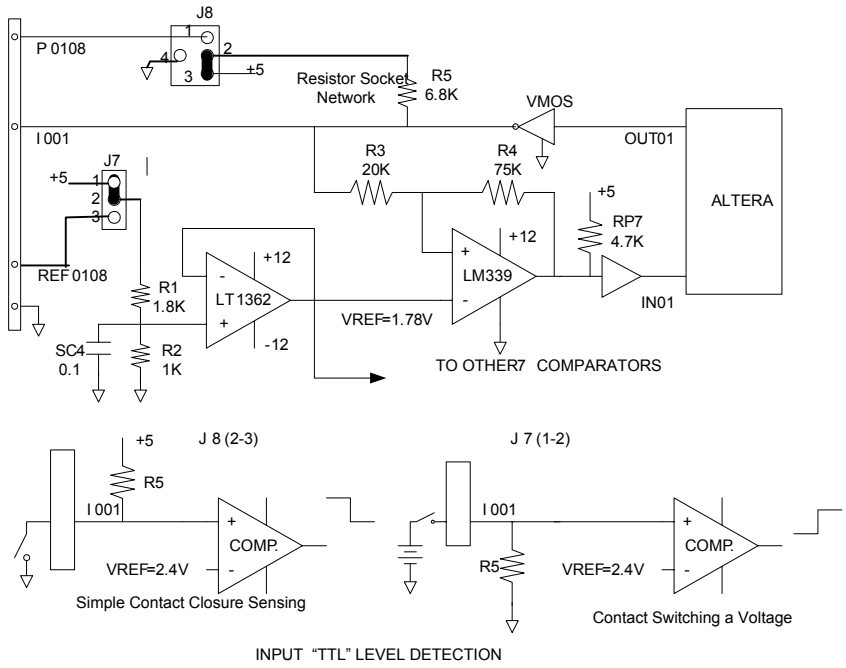
By default J7 is installed pin 1-2. In this case, the local +5V is used as internal reference. It is divided by R1 (1.8 kΩ) and R2 (1 kΩ) and provides a +1.8 V threshold.

External Reference:

J7 is installed pin 2-3. A voltage (VREF) is connected between the reference ground and the input reference line REF0108 (External Voltage provided).
The threshold reference will be: THRESHOLD = (VREF * R2) / (R1 +R2).
For example if VREF is +28V then the threshold is +10Volts which is the maximum allowed.

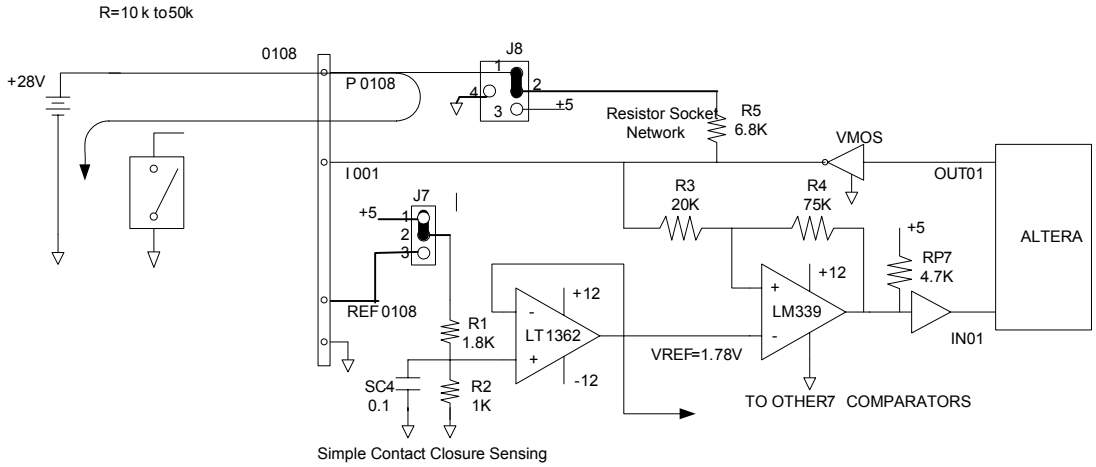
5.3.1 EXAMPLE #1: INPUT SIGNAL with “TTL” levels.

J7 pin 1-2 Threshold level is +2.4V
J8 pin 2-3 I/O is an input, R5 (6.8 kΩ on socket) is used as pull-up.
If there is no connection to the I/O line the signal appears as “1”.

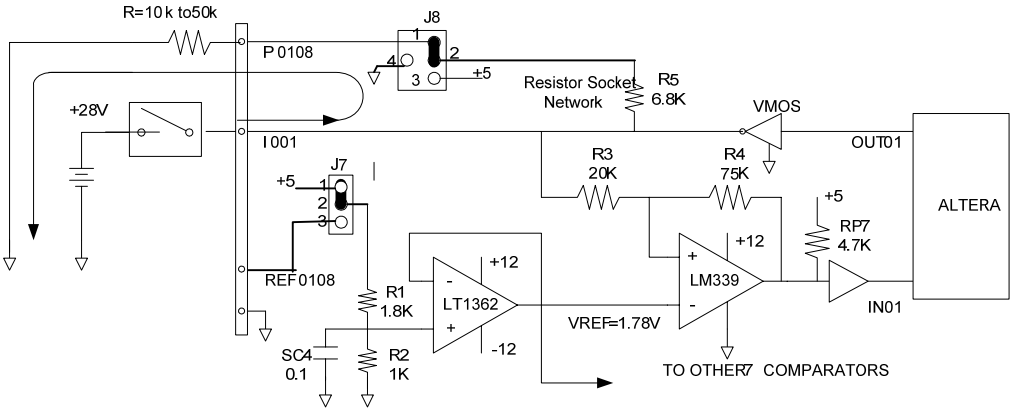


5.3.2 EXAMPLE #2: INPUT SIGNAL up to +28Volts.

J11 installed External pull-up
J12 installed Threshold level is +2.4v
J13 (none) I/O IS input, R5 (4.7 kΩ on socket) is used as pull-up but an additional resistance is necessary to keep the power dissipation of R5 below 1/8 W (it would be 0.17 W without additional resistor).
If there is no connection to the I/O line the signal appears as “1”.



Simple Contact Closure Sensing

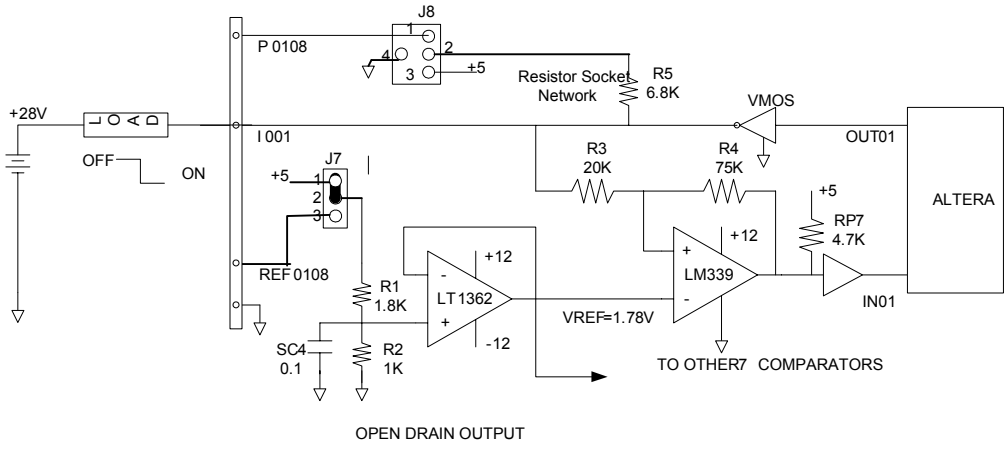


Contact Switching a Voltage

5.3.3 EXAMPLE #3 : OPEN DRAIN OUTPUT SIGNAL .

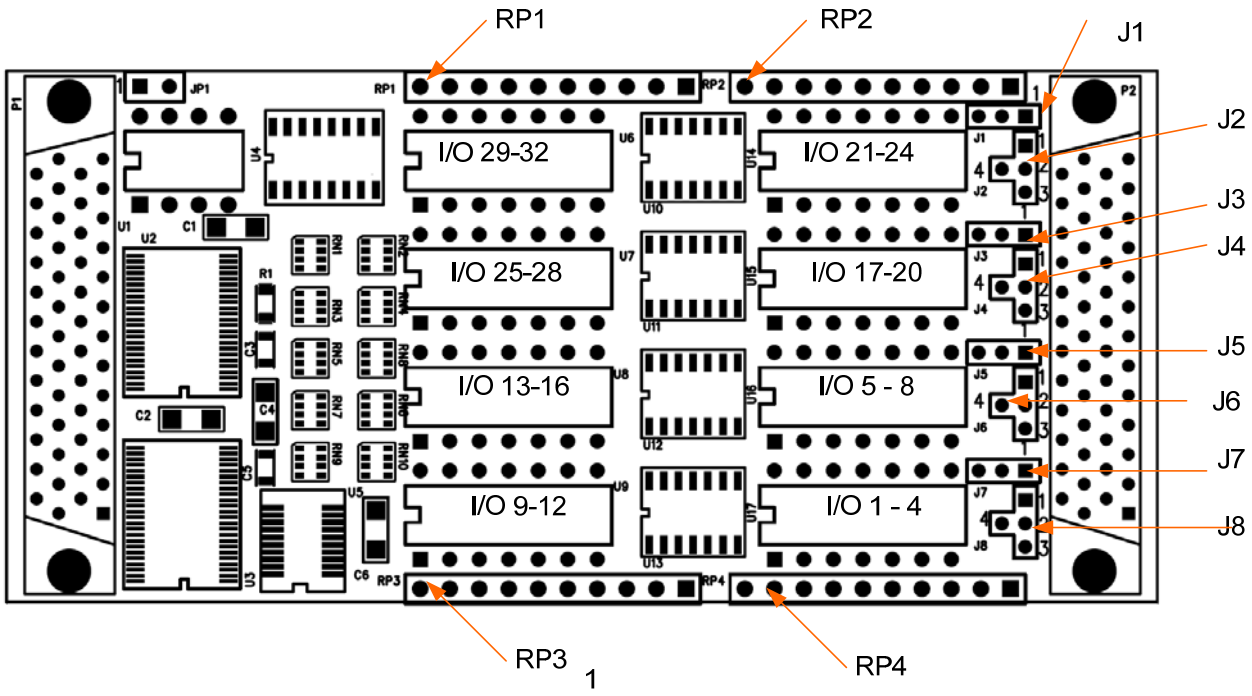
J8 (NONE) No pull-up
J7 (1-2) Threshold level is +2.4V

Note: The output signal can be “read back”

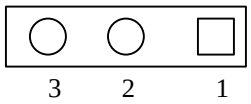


6 CONNECTORS AND JUMPERS

The connector and jumpers placement is depicted below.



6.1 Voltage Reference selection jumpers

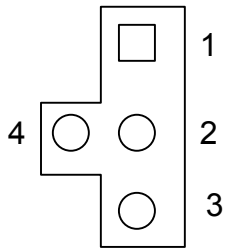


PORT	Jumper Location	+5V threshold Reference	External threshold Reference	Factory Default
1-8	J7	1-2	2-3	1-2
9-16	J5	1-2	2-3	1-2
17-24	J3	1-2	2-3	1-2
25-32	J1	1-2	2-3	1-2

6.2 Pull-up selection jumpers

The pull-up resistors are in Group of eight (8)

RP4 : Pullup Network 6.8K For I0# 01 – 08
RP3 : Pullup Network 6.8K For I0# 09 – 16
RP1 : Pullup Network 6.8K For I0# 17 – 24
RP2 : Pullup Network 6.8K For I0# 25 – 32



PORT	Jumper Location	PULL-UP +5V	PULL-DOWN GND	External Pull-up voltage	FACTORY DEFAULT
1-8	J8	2-3	2-4	1-2	2-3
9-16	J6	2-3	2-4	1-2	2-3
17-24	J4	2-3	2-4	1-2	2-3
25-32	J2	2-3	2-4	1-2	2-3

